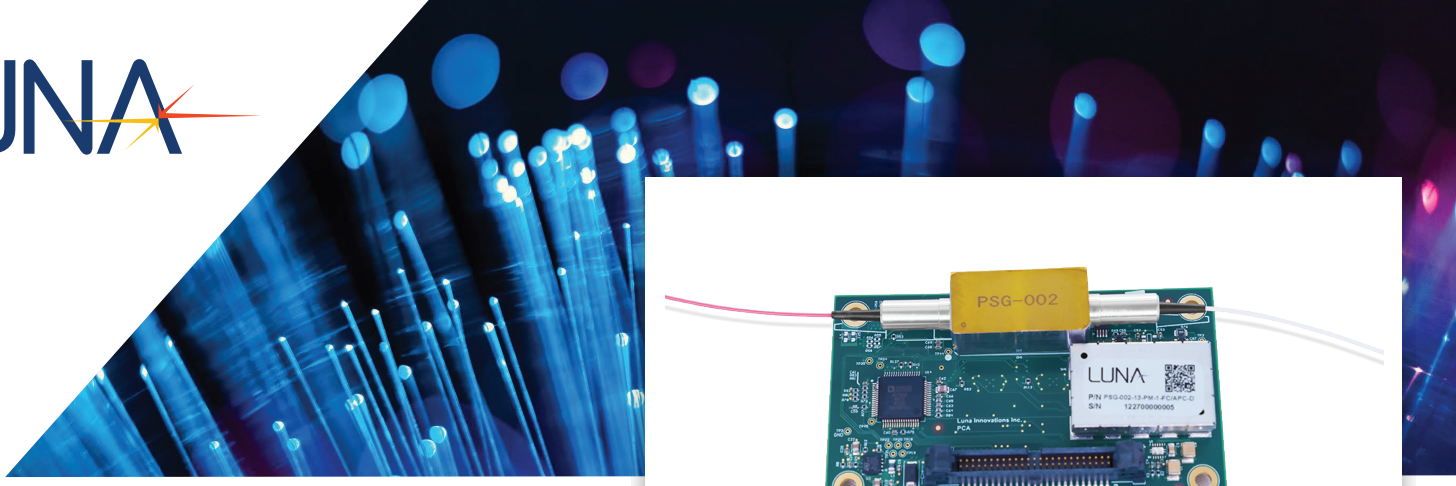

PSG-002-D

High-Speed Polarization State Generator

LUNA's high-speed polarization state generator (PSG) module generates any of six distinct states of polarization (SOP) on the Poincaré Sphere in less than 50µs, with a repeatability better than 0.1°. This compact module is easy to control and requires very little power, making it ideal for integration into systems that require precise generation of polarization basis states. The PSG is easily controlled with a 4-bit TTL signal either from a microcontroller or a computer

Optical Connections

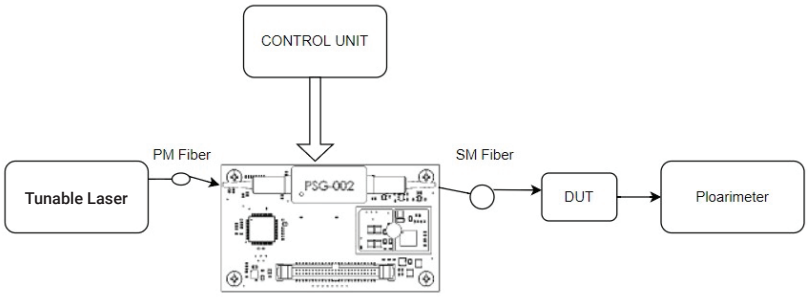

Figure 1 Application Example - Swept Wavelength Polarization Measurement

KEY FEATURES

- Switches between 6 Polarization States: LCP, RCP, Linear ±22.5°, Linear ±67.5°
- Typical Switching Time 45 µs
- SOP Repeatability 0.1°
- Self-Latching
- Zero Static Power Dissipation
- 4-bit Control
- Compact
- Minimal Heat Generation

APPLICATIONS

- Polarization OTDR
- Polarization Rotation
- Mueller Matrix-based Polarization Analysis
- Swept-Frequency Measurement
- Qauntum Communications

High-speed polarization state generator (PSG) with six distinct states of polarization (SOP)

PINS DESCRIPTION

Table 1: J1 connector on Board Pins Function Descriptions		
1	+12V	PSG optical head drive circuit power supply >1000mA (pin +pin2)
2	+12V	PSG optical head drive circuit power supply >1000mA (pin +pin2)
3	GND	System ground
4	GND	System ground
5	SPI1_CTRL_SCLK	SPI1 Clock Signal. Maximum clock frequency is 10 MHz.
6	SPI1_CTRL_0	Used together with SPI1_CTRL_1 and SPI1_CTRL_2 to control the output of an SNX4HC138 decoder (component U8). The output of component U8 is used for determining which chip is selected for communication on the SPI1 lines.
7	SPI1_CTRL_MOSI	SPI Master Output Slave Input. Used for moving data from an SPI master into an SPI slave peripheral.
8	C_N	SPI Master Output Slave Input. Used for moving data from an SPI master into an SPI slave peripheral.
9	D_P	SPI Master Input-Slave Output. Used for moving data from an SPI slave peripheral into an SPI master.
10	D_N	Used together with SPI1_CTRL_0 and SPI1_CTRL_1 to control the output of an SNX4HC138 decoder (component U8). The output of component U8 is used for determining which chip is selected for communication on the SPI1 lines.

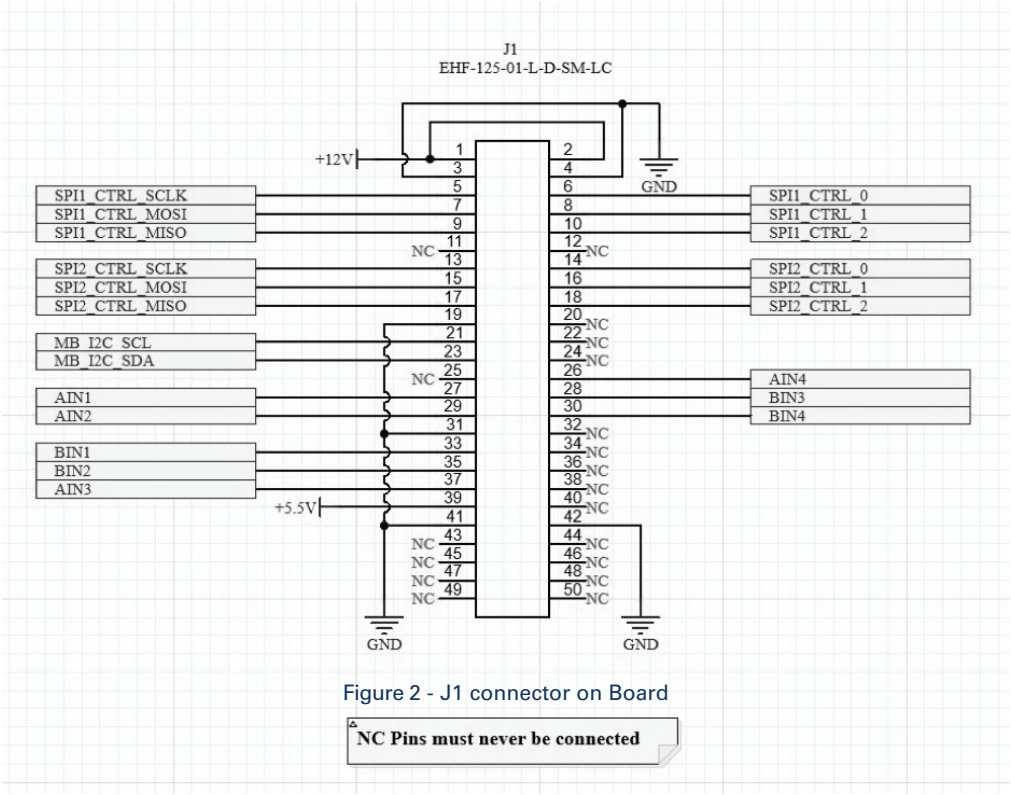

Figure 2 - J1 connector on Board

Pin #	Mnemonic	Description
11	NC	Dangling. cannot be connected to any circuit
12	NC	Dangling. cannot be connected to any circuit
13	SPI2_CTRL_SCLK	SPI2 Clock Signal. Maximum clock frequency is 10 MHz.
14	SPI2_CTRL_0	Used together with SPI2_CTRL_1 and SPI2_CTRL_2 to control the output of an SNX4HC138 decoder (component U9). The output of component U9 is used for determining which chip is selected for communication on the SPI2 lines.
15	SPI2_CTRL_MOSI	SPI Master Output Slave Input. Used for moving data from an SPI master into an SPI slave peripheral.
16	SPI2_CTRL_1	Used together with SPI2_CTRL_1 and SPI2_CTRL_2 to control the output of an SNX4HC138 decoder (component U9). The output of component U9 is used for determining which chip is selected for communication on the SPI2 lines.
17	SPI2_CTRL_MISO	SPI Master Input-Slave Output. Used for moving data from an SPI slave peripheral into an SPI master.
18	SPI2_CTRL_2	Used together with SPI2_CTRL_1 and SPI2_CTRL_2 to control the output of an SNX4HC138 decoder (component U9). The output of component U9 is used for determining which chip is selected for communication on the SPI2 lines.
19	GND	System ground
20	NC	Dangling. cannot be connected to any circuit
21	MB_I2C_SCL	I2C Serial Clock. Maximum clock frequency is 400 kHz with a 33% duty cycle.
22	NC	Dangling. cannot be connected to any circuit
23	MB_I2C_SDA	I2C Serial Data.
24	NC	Dangling. cannot be connected to any circuit
25	NC	Dangling. cannot be connected to any circuit
26	AIN4	AIN3 and AIN4 are used for controlling the state of the C+ pin (pin 7) and the C- pin (pin 8) of the PSG optical head.
27	AIN1	AIN1 and AIN2 are used for controlling the state of the A+ pin (pin 1) and the A- pin (pin 2) of the PSG optical head.
28	BIN3	BIN3 and BIN4 are used for controlling the state of the D+ pin (pin 9) and the D- pin (pin 10) of the PSG optical head.
29	AIN2	AIN1 and AIN2 are used for controlling the state of the A+ pin (pin 1) and the A- pin (pin 2) of the PSG optical head.
30	BIN4	BIN3 and BIN4 are used for controlling the state of the D+ pin (pin 9) and the D- pin (pin 10) of the PSG optical head.
31	GND	System ground
32	NC	Dangling. cannot be connected to any circuit
33	BIN1	BIN1 and BIN2 are used for controlling the state of the B+ pin (pin 3) and the B- pin (pin 4) of the PSG optical head.
34	NC	Dangling. cannot be connected to any circuit
35	BIN2	BIN1 and BIN2 are used for controlling the state of the B+ pin (pin 3) and the B- pin (pin 4) of the PSG optical head.

Pin #	Mnemonic	Description
36	NC	Dangling. cannot be connected to any circuit
37	AIN3	AIN3 and AIN4 are used for controlling the state of the C+ pin (pin 7) and the C- pin (pin 8) of the PSG optical head.
38	NC	Dangling. cannot be connected to any circuit
39	+5.5V	Control circuit power supply >200mA
40	NC	Dangling. cannot be connected to any circuit
41	GND	System ground
42	GND	System ground
43	NC	Dangling. cannot be connected to any circuit
44	NC	Dangling. cannot be connected to any circuit
45	NC	Dangling. cannot be connected to any circuit
46	NC	Dangling. cannot be connected to any circuit
47	NC	Dangling. cannot be connected to any circuit
48	NC	Dangling. cannot be connected to any circuit
49	NC	Dangling. cannot be connected to any circuit
50	NC	Dangling. cannot be connected to any circuit

SPI1 Chip Selection Table

SPI1_CTRL_0	SPI1_CTRL_1	SPI1_CTRL_2	SPI1_CTRL_0	SPI1_CTRL_1	SPI1_CTRL_2	Chip Selected
1	0	0	X	X	X	Conditions Monitor ADC U14
0	1	0	X	X	X	I/O Expander U8

SPI2 Chip Selection Table

SPI1_CTRL_0	SPI1_CTRL_1	SPI1_CTRL_2	SPI1_CTRL_0	SPI1_CTRL_1	SPI1_CTRL_2	Chip Selected
1	1	0	X	X	X	I/O Expander U9
X	X	X	0	1	0	Flash Memory U15

RECOMMEND OPERATING CONDITION

Table 2: Recommended operating conditions

Attribute	Min	Typical	Max	Unit
Power supply pin voltage	11	12	15	V
Logic pin voltage	0	5	5.5	V
Logic pin signal pulse width	50	80	1000	μs
Operating temperature range	0	25	50	°C
Input fiber		PM		
Output fiber		SM		

H-BRIDGE CONTROL

Table 3: H-bridge Control				
Description	**A_IN**	**B_IN**	**OUT1**	**OUT2**
Coast; H-bridge disabled to High-Z (sleep entered after 1 ms)	0	0	High-Z	High-Z
Reverse (Current OUT2 -> OUT1)	0	1	L	H
Forward (Current OUT1 -> OUT2)	1	0	H	L
Brake; low-side slow decay	1	1	L	L

POLARIZATION STATE AND ANGLE DEFINITIONS

Electrical field rotation directions and angles are defined below when observed against the direction of propagation.

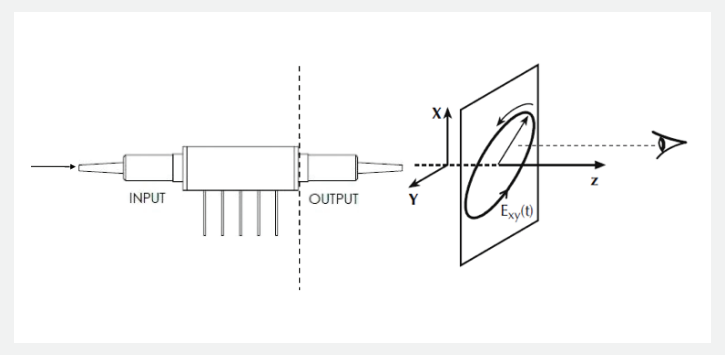

Figure 2 Electrical field is observed against the direction of propagation.
Output SOPs are defined at the plane marked by the vertical dotted line at the output end of the PSG frame, before the output pigtail.

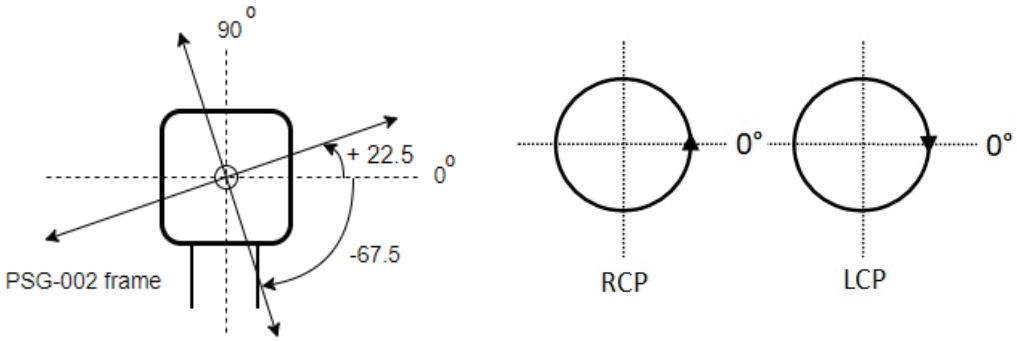

Figure 3 Polarization state and rotation direction definitions

Definitions in 3:

RCP – Right Circular Polarization State
LCP – Left Circular Polarization State
L + θ – Linear Polarization State with positive angle
L – θ – Linear Polarization State with negative angle
θ = 22.5° or 67.5°

Linear polarization angles are defined relative to the horizontal axis.

SPECIFICATIONS

Specifications apply at ambient temperature T = 23°C and at center wavelength, unless otherwise noted. Unless otherwise noted, electrical parameters are given for a single polarization switch, driven with an H-Bridge circuit with the specified bias voltages applied to the switches.

Table 4: Absolute Maximum Rating			
Parameter	**Min**	**Max**	**Unit**
Optics			
Optical input power	300		mW
Electronics			
Operating voltage (DC)	12 ± 1.0		V
Quiescent current	5		mA
Operating current (Alternating switching frequency 8KHz)		50	mA
Maximum transient current (<1us)		160	mA
Pulse width			

NOTES:

1. Maximum allowed instantaneous current during a drive pulse.
2. The pulse width at which the maximum instantaneous current may reach 150 mA. Exceeding this value may cause higher than normal device heating or damage the switches.

Table 5: Physical Operating Conditions			
Parameter	**Min.**	**Max.**	**Unit**
Operating Temperature	0	50	°C
Storage Temperature	-40	85	°C

Table 6: Optical Characteristics				
Parameter	**Min.**	**Typical**	**Max.**	**Unit**
Operation Wavelength[1]				
C band	1480	1550	1620	nm
O band	1260	1310	1340	nm
Insertion Loss[2]				
C band			1.0	dB
O band			1.2	dB
State Dependent Loss (ΔIL over all SOPs at fixed wavelength)			0.1	dB
Wavelength Dependent Loss (ΔIL over all wavelengths at fixed SOP)			0.3	dB
Return Loss			-55	dB
SOP Relative Angle Accuracy (Deviation from 90° of angle between output SOPs on Poincaré Sphere)[3,4]			+/- 10	dB
SOP Repeatability (on Poincaré Sphere)[3]		±0.1		deg
SOP Accuracy to Target (on Poincaré Sphere at λc and 23°C[1,3]			±5	deg
Rotation Angle Wavelength Dependence[5]				
1550nm		-0.068		deg/nm
1310nm		-0.091		deg/nm
Rotation Angle Temperature Dependence[5]				
1550nm		-0.084		deg/ °C
1310nm		-0.11		deg/ °C
SOP Switching Time[6]				
At bias voltage 10V	40	45	50	µs
At bias voltage 5V	70	80	100	µs
At bias voltage 3.3V	90	120	150	µs
Optical Power Handling			300	mW

NOTES: Values are referenced without connectors:

1. Center wavelength λc =1550 or 1310nm. For 1550nm version, calibrated wavelength range 1500-1580nm and operating wavelength range 1480-1620nm standard. For 1310nm version, calibrated range = operating wavelength range (1260-1340nm). Contact Luna Innovations regarding other wavelength options. The switch rotation angles, and therefore the output SOPs, are closest to ideal values at center wavelength and room temperature. Calibration parameters are provided for users to calculate the actual output SOPs at different temperatures and wavelengths. Measurements taken over the calibrated wavelength range are used to determine the calibration parameters for each PSG.
2. With input polarization aligned to polarizer transmission axis.
3. Relative angles on the Poincaré sphere are twice the electrical field rotation angles in real space.
4. Over all wavelengths and temperatures in the operational ranges.
5. Wavelength and temperature dependence of the relative angle between adjacent linear SOPs, in real space. A negative sign denotes that the angle decreases with increasing wavelength or temperature. Wavelength dependence tested at room temperature. Temperature dependence tested at λc.
6. Time interval between drive signal pulse leading edge and completion of SOP transition (t_5 and t_7 in Figure 7) at room temperature (~23°C) using an H-bridge driver circuit.

TIMING CHARACTERISTICS

Table 7: Timing Parameter Labels and Definitions*

Definitions	Min.	Typical	Max.	Timing Symbol	Test Conditions
Drive Pulse Signal With. t_1 is for positive signal, t_3 is for negative signal.	50 80	80 100	1000 1000	t_1, t_3	$20 < t_2 < 500$
Drive Pulse Signal Interval	20	50	N/A	t_2	$t_2 > 500$
SOP Switch Delay Time	20	25	30	t_4, t_6	
SOP Switch Time	40	45	50	t_5, t_7	

* All values in μs

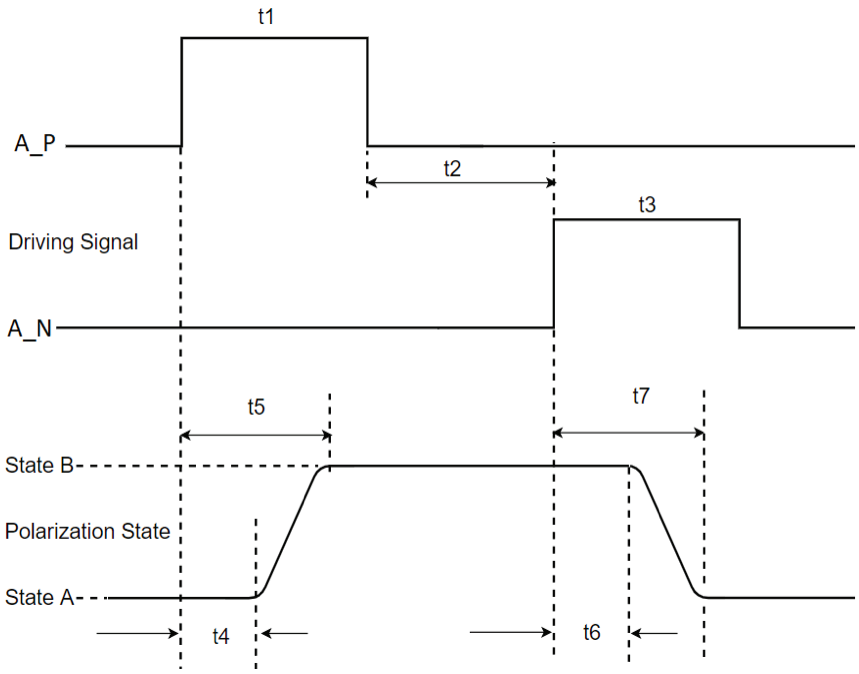

Figure 4 Polarization response to drive signal

THERMOGENESIS

This section describes the heating effects that can be expected due to operation of the PSG-002. The operational temperature elevation refers to the amount the device temperature can be expected to rise (relative to ambient temperature) due to device operation. It is dependent on the drive conditions used for switching, the number of switches toggled simultaneously, and the switching frequency.

Table 8 Internal temperature elevation (relative to ambient temperature)		Operational Temperature Elevation		
Drive Conditions[1]	**Unit**	**Min.**	**Typical**	**Max.**
Worst Case[2]	°C		10	
Typical Operation[3]	°C		3	

NOTES:

1. Data in this table was measured at room temperature ambient, with drive pulse width and interval between pulses both equal to 50µs, using an H-bridge driver circuit with bias voltage 10V.
2. Worst Case: The largest operational temperature increase occurs when all 4 bits are switched simultaneously and continuously.
3. Typical Operation: a more typical operation condition is to cycle the SOP sequentially through the 6 distinct polarization states (LCP, L+22.5, L+67.5, L–67.5, L–22.5, RCP).

TEMPERATURE SENSOR

Table 9: Thermal Sensor Specifications						
Parameter	**Symbol**	**Condition**	**Min.**	**Typical**	**Max.**	**Unit**
Nominal Resistance at 0 °C	R_0	Pt1000	999.8	1000	1001.2	Ω
Tolerance at 25 °C			-0.43	0	0.43	°C
Temperature Coefficient of Resistance	TCR	0 °C, 100 °C		3850		ppm/°C
Temperature Range			-50		600	°C
Measuring Current R_0: 1000Ω					0.4	mA

The RTD Pt1000 resistance to temperature (R/T) conversion can be calculated using the following equation, where the value of parameter a is 3.8679E-03.

$$R_{(T)} = R_{(0)} \times (1 + a \times T) \qquad \text{Equation 1}$$

Using Equation 1, the maximum error for the R/T conversion is ± 3Ω.

PRINCIPLE OF OPERATION

The PSG-002 uses a series of 4 electrically controlled, self-latching polarization switches in combination with free space optics to change its output polarization state. The device can generate 6 distinct states of polarization (SOP): linear polarization states oriented at –22.5°, +22.5°, –67.5°, and +67.5° relative to the horizontal axis, as well as right hand circular (RHC) and left hand circular (LHC) polarization states. These SOPs are defined at the ou put edge of the PSG-002 frame, just before the light enters the output pigtail, as shown in Figure 4 and Figure 5.

The PSG-002 has an internal polarizer situated at the input side of the frame, just after the input pigtail. The input pigtail fiber can be SM or PM. If the input fiber is PM, its slow axis is aligned to the transmission axis of the polarizer. Note that because of the polarizer, the device loss will be higher if the input light is unpolarized or is not aligned to the polarizer transmission axis (e.g. if the input pigtail is SM fiber). In addition, polarization fluctuation at the input will cause power fluctuations at the output.

The birefringence of the output SM fiber can cause polarization rotation, so the absolute SOPs measured at the end of the output pigtail are generally different from the SOPs at the edge of the frame; however, the angular relationship between the SOPs remains the same. The 6 generated polarization states are still symmetrically distributed on the Poincaré sphere.

With 4 binary switches, there are 16 possible logic states. Each logic state corresponds to a particular output polarization state, but only 6 of the 16 polarization states are unique; the others are degenerate. The table below shows the logic states and their corresponding polarization states.

Table 10 PSG-002 logic states and corresponding output polarizations (before output pigtail)

State		BIT	4	3	2	1.	State		BIT	4	3	2	1.
#	SOP	SW	A	B	C	D.	#	SOP	SW	A	B	C	D.
0	LCP		-	-	-	-	8	L+22.5		+	-	-	-
1	LCP		-	-	-	+	9	L−67.5		+	-	-	+
2	LCP		-	-	+	-	10	L−67.5		+	-	+	-
3	LCP		-	-	+	-	11	L−22.5		+	-	+	+
4	L+22.5		-	+	-	-	12	RCP		+	+	-	-
5	L+67.5		-	+	-	+	13	RCP		+	+	-	+
6	L−67.5		-	+	+	-	14	RCP		+	+	+	-
7	L−22.5		-	+	+	+	15	RCP		+	+	+	+

NOTES:

"+" indicates a positive switch rotation angle (drive pulse applied to its positive rotation pin) and corresponds to logic level 1 for that bit. "–" indicates a negative switch rotation angle (drive pulse applied to its negative rotation pin) and corresponds to logic level 0 for that bit. See Figure 5 for rotation angle frame of reference.

Calibration Parameters

The output SOPs listed in Table 10 are ideal (target) states. The actual output SOP for a particular logic state is wavelength and temperature dependent. In addition, individual switch variations cause minor deviations from ideal values. To account for these effects, each PSG module comes with a set of calibration parameters derived from measurements of the actual output SOPs at all logic states at different wavelengths and temperatures. These calibration parameters can be used with the following formulas to calculate the actual output SOP (at the exit plane before the output pigtail) corresponding to each logic state of a particular PSG, at a particular wavelength and temperature. Once the SOPs at the exit plane are known, it is possible to calculate the transfer matrix of the output optical fiber or other components along the optical path.

The SOP at the PSG output port just before the pigtail fiber is given by:

$$SOP = \begin{pmatrix} 1 \\ -cos2\alpha cos2\beta + sin2\alpha sin2\beta cos\gamma \\ -cos2\alpha sin2\beta - sin2\alpha cos2\beta cos\gamma \\ sin2\alpha sin\gamma \end{pmatrix}$$

Where

$$\alpha = \sum_{n=3}^{4} (Bit_n f_n + (Bit_n - 1) g_n)$$

$$\beta = \sum_{n=1}^{2} (Bit_n f_n + (Bit_n - 1) g_n)$$

$$f_n = \theta + b_n + a_n(\lambda - \lambda_c) + (h_1(\lambda - \lambda_c) + h_2) \cdot (T - T_0)$$

$$g_n = \theta + d_n + c_n(\lambda - \lambda_c) + (h_1(\lambda - \lambda_c) + h_2) \cdot (T - T_0)$$

When n = 1, 3, 4, θ=22.5. When n = 2, θ=45.

λc is the center wavelength for the PSG, in nm (e.g. 1550).

$$\gamma = \gamma_0 + h_3(T\text{-}T_0)$$

T is the temperature inside the PSG module (in °C). It can be determined by measuring the resistance between pins T1 and T2 (see PIN CONFIGURATIONS section). The conversion between resistance and temperature is described in the TEMPERATURE SENSOR section. The temperature inside the PSG module is approximately equal to T_0 at an ambient temperature of 25°C.

a_n, b_n, c_n, d_n, γ , h_1, h_2 , h_3 and T_0 are the calibration parameters provided with each PSG-002. Table 11 shows an example the calibration parameters.

Table 11 An example of the calibration parameters

n	a_n	b_n	c_n	d_n
1	-0.0349	0.0021	-0.0355	0.0743
2	-0.0699	-0.0037	-0.0711	0.1407
3	-0.0311	0.3732	-0.0343	-0.1022
4	0.0311	0.3732	-0.0343	-0.1022
T_0 (°C)	25.84			
Γ_0 (-deg)	90.12			
h_1	$4.85X10^{-2}$			
h_2	-0.0456			
h_3	0			

Bit_n is the logic level (1 or 0) of the n^{th} control bit. 1 = positive (+) switch rotation angle and 0 = negative (–) rotation angle in Table 2. Bit 4 (switch A) is the most significant bit (MSB). For example, for logic state 12 (1 1 0 0), Bit_n values (n = 4, 3, 2, 1) are:

Bit_4 = 1 (switch A rotation +)

Bit_3 = 1 (switch B rotation +)

Bit_2 = 0 (switch C rotation –)

Bit_1 = 0 (switch D rotation –)

DIMENSIONS

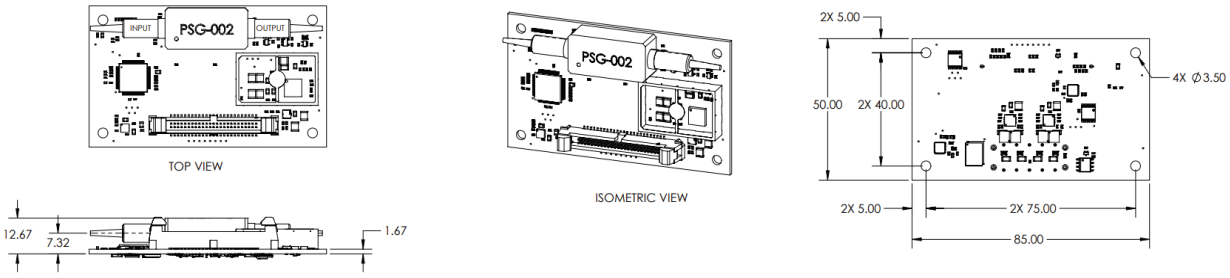

Figure 5 Mechanical drawing and dimensions (in mm)

ORDERING INFORMATION

P/N	Description
PSG-002-15-PM-1-FC/APC-D	Polarization state generator optical head with driver board, 1550nm, PM input, SM output, 1 m pigtails (typical), FC/APC connectors
PSG-002-13-PM-1-FC/APC-D	Polarization state generator optical head with driver board, 1310nm, PM input, SM output, 1 m pigtails (typical), FC/APC connectors

REVISION HISTORY

Revision	Date	Note
1.0	9/1/2022	Original document

+1.866.586.2682
solutions@lunainc.com
www.lunainc.com